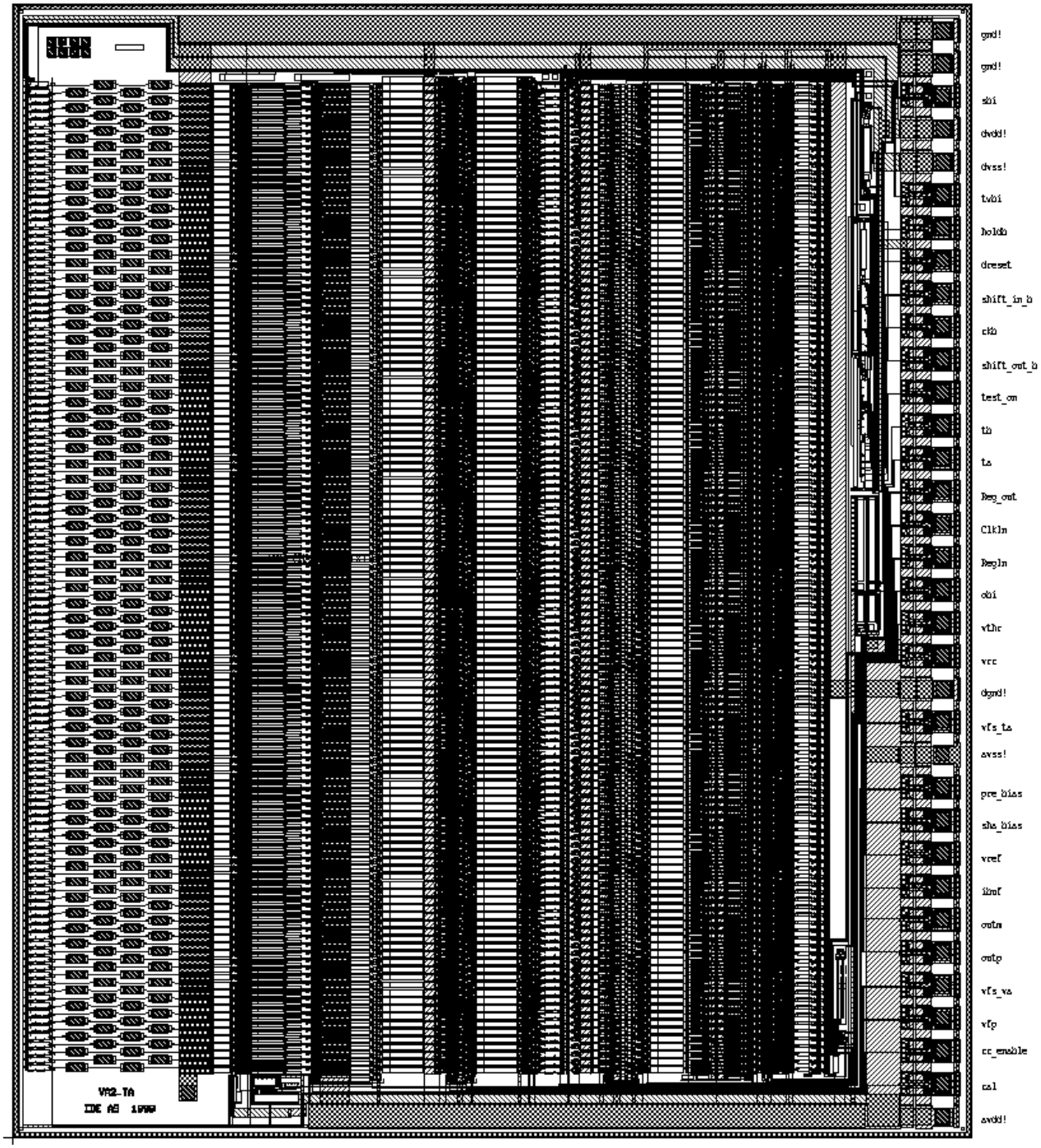
Integrated
Detector &
Electronics AS

VA2_TA



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The chip consists of two parts: a VA2 and a TA chip.

The VA2 is a 128-channel low-noise/low-power charge sensitive preamplifier-shaper, with sample/hold, multiplexed analogue readout and calibration facilities. This part of circuit offers full parallel readout of all 128 preamplifiers, which makes the chip compatible with the TA. The VA2 offers also input leakage current compensation automatically adjusted in each preamplifier channel.

The TA is a 128-channel low power fast triggering ASIC to be used with VA2 in the front. This part of VA2_TA includes for each channel a fast CR-RC shaper followed by a level-sensitive discriminator. The trigger signals from each channel are wire-or'ed together onto on common trigger output.

The chip was produced in the AMS 1.2µm CMOS CAE process and should be powered the following way:

Name	Description	Nom. Value
AVDD	Analogue positive voltage supply	+2V
AVSS	Analogue negative voltage supply	-2V
GND	Signal ground	0V
DVDD	Digital positive voltage supply	+2V
DVSS	Digital negative voltage supply	-2V

Table 1: Power-supplies

Chip Architecture

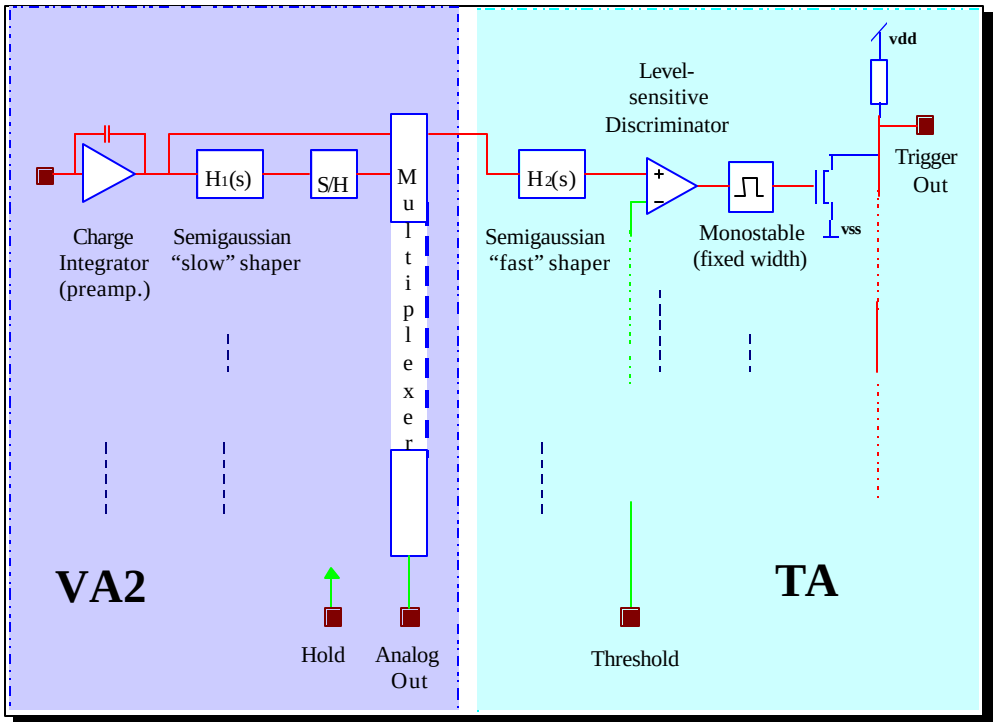

Figure 1, Principle of the VA2_TA

Pad Description

The output, control and power pads are listed below from top to bottom (see chip plot on first page).

Pad name	Type	Description	Nominal value
gnd	p	Signal ground	0V
sbi	ai	Bias-current for shaper (TA)	70µA
dvdd	p	Digital VDD	+2V
dvss	p	Digital VSS	-2V
twbi	ai	Bias adjust for trigger width	10µA
holdb	di	Used to hold analogue data	Logical
dreset	di	Reset of digital part	Logical
shift_in_b	di	Start pulse for read-out	Logical
ckb	di	Clock for read-out register	Logical
shift_out_b	do	Signalling end of read-out	Logical
test_on	di	Turns chip into test-mode	Logival
tb	ao	Trigger out inverted	Current
ta	ao	Trigger out	Current
Reg_out	do	Output of the disable register	Logical
ClkIn	di	Clock input for disable register	Logical
RegIn	di	Input to the disable register	Logical
obi	ai	Bias-current for Discriminator	120µA
vthr	ai	Discriminator threshold	± 100mV
vrc	ai	Control voltage for High-pass filter resistor (NMOS) in shaper (TA)	1.4V
dgnd	p	Signal ground	0V
vfs-ta	ai	Control voltage for feedback resistor (NMOS) in shaper (TA)	0.6V
avss	p	Analogue VSS	-2V
pre_bias	ai	Bias-current for preamplifier	500µA
sha_bias	ai	Bias-current for shaper (VA2)	22µA
vref	ai	Not in use (recommended to decoupling capacitor)	
ibuf	ai	Bias-current for output-buffer	
outm	ao	Negative output signal	Current
outp	ao	Positive output signal	Current
vfs_va	ai	Control voltage for feedback resistor (NMOS) in shaper (VA2)	0.4V
vfp	ai	Control voltage for feedback resistor (NMOS) in preamplifier	-0.35V
cc_enable	di	Leak-current compensation ON	Logical
cal	ai	Test input signal	1 MIP
avdd	p	Analogue VDD	+2V

p = power, di = digital in, do = digital out, ai = analogue in, ao = analogue out
Logical = +2V (“1”) / -2V (“0”)

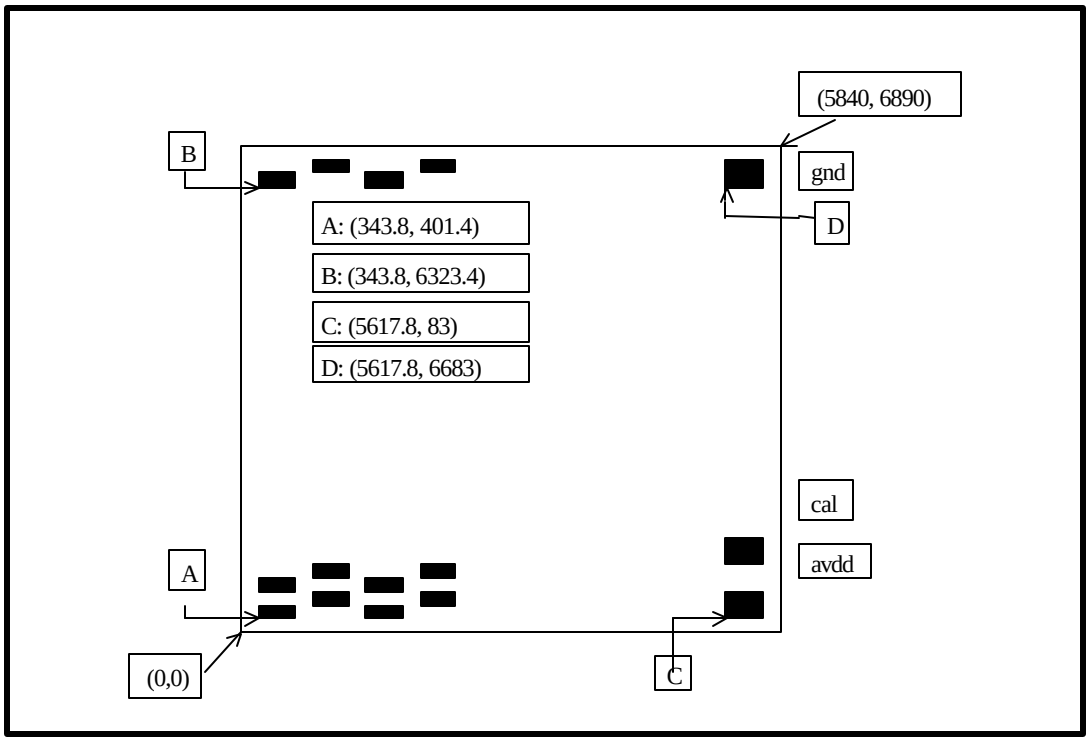

Figure 2, Chip geometry & pad placement (Not to scale - all dimensions in µm. Please note that the referred co-ordinates are layout co-ordinates. Add 50-100 µm on each side for scribe/cutting tolerances).

- Input pads:

  Pad size: 90 µm x 50 µm
  Pad pitch: 94 µm
  Row pitch: 170 µm

- Output, control and power pads:

  Pad size: 90 µm x 90 µm
  Pad pitch: 200 µm

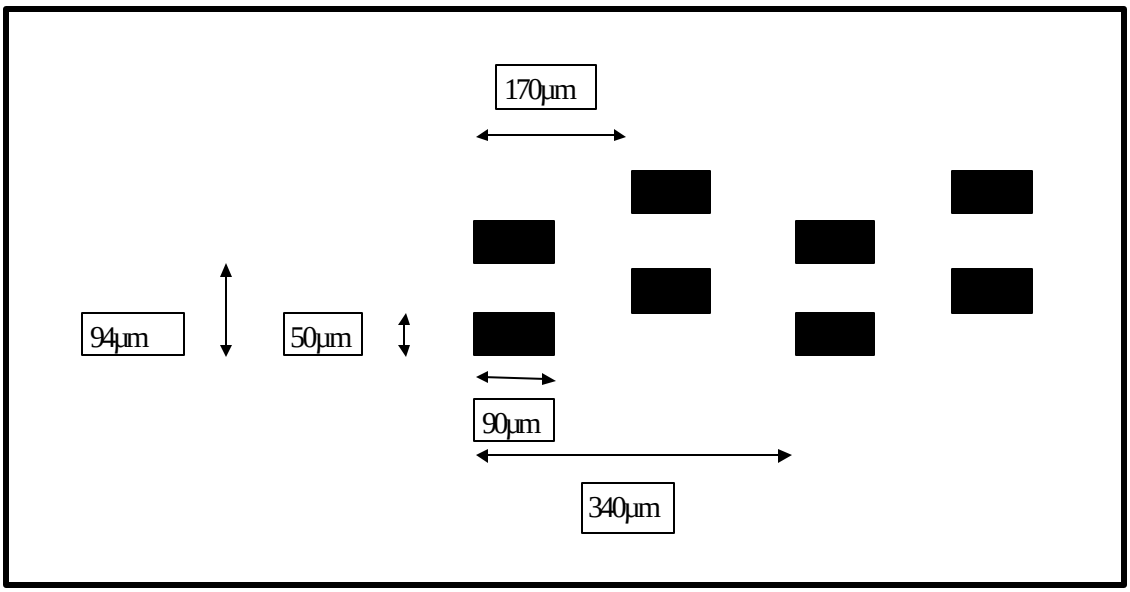

Figure 3, Definition of input pad size and pitch.